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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,227	12/05/2003	In-Su Kim	20061/OF03P196	9222

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,227	KIM	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/05/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/729,227. Currently, claims 1-7 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. *Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagatani et al. (US 6,716,718 B2) in view of Zheng et al. (US 6,734,082 B2).*

The Nagatani et al. patent (Nagatani) discloses a method of manufacturing a semiconductor device (figs. 1-12 and accompanying text). The method comprises: forming a multi-layered insulating structure on a semiconductor substrate 1, wherein the multi-layered insulating structure comprises pad oxide layer 2, polysilicon layer 3, and silicon nitride layer 4 (fig.1 and col. 4, lines 31-38);[1] forming an opening in the insulating structure to expose a field region of the semiconductor substrate (fig. 2 and col. 4, lines 39-53); forming a trench 6 in the field region of the semiconductor substrate (fig. 3 and col. 4, lines 54-60); forming a groove on an edge portion of the

[1] Presumably, the polysilicon layer 3 is formed of intrinsic polysilicon, since there is no mention of the polysilicon layer being doped either *in situ* or in a subsequent processing step. In the

intermediate layer 3a of the multi-layered insulating structure (fig. 4 and col. 4, lines 61-67); forming a liner insulating layer 7 in a desired thickness on a surface of the multi-layered insulating structure (figs. 5, 6, and col. 5, lines 1-9); and filling the groove and the trench with an oxide layer 8 (fig. 7 and col. 5, lines 17-18). As shown in figs. 5 and 6, the liner insulating layer 7 is formed along the groove and the trench, as recited in claim 2. The liner insulating layer 7 is formed of a liner oxide layer, as recited in claim 3 (col. 5, lines 1-9).

Nagatani lacks anticipation only in not teaching that the liner insulating layer 7 is deposited on a surface of the multi-layered insulating structure, as recited in claim 1, or that the liner insulating layer 7 is deposited using an atomic layer deposition process, as recited in claim 4. Instead, the liner insulating liner 7 is formed by a thermal oxidation method. The Zheng et al. patent (Zheng) discloses a method of manufacturing a semiconductor device (figs. 1-7 and accompanying text). The method, which is similar to that of Nagatani, comprises: forming a multi-layered insulating structure on a substrate 2, the multi-layered structure comprising oxide layer 3 and nitride layer 4 (fig. 1 and col. 3, lines 21-29). The method further comprises: forming an opening in the insulating structure, and forming a trench 5 in the substrate (fig. 1 and col. 3, lines 29-34); forming a groove on an edge portion of the multi-layered insulating structure (fig. 3 and col. 3, lines 54-57); forming a liner oxide layer 9 to a desired thickness on a surface of the multi-layered insulating

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instance when polysilicon layer 3 is formed of intrinsic polysilicon, polysilicon layer 3 is an

structure using an ALD process (fig. 4 and col. 3, line 62 - col. 4, line 4). As in Nagatani, the trench is subsequently filled with an oxide layer 13 (fig. 5 and col. 4, lines 21-27). The liner oxide layer 9 is deposited at a temperature of approximately 250°C to 350°C, as recited in claim 6 (col. 4, lines 4-7).

Since Nagatani and Zheng are from the same field of endeavor - methods of making shallow trench isolation structures in semiconductor devices - the purpose for which Zheng is relied upon would have been recognized in the pertinent reference of Nagatani by one of ordinary skill in the art at the time the invention was made.

As discussed above, the liner insulating layer 7 is formed on a surface of the multi-layered insulating structure using a thermal oxidation process. It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify Nagatani by forming the liner insulating layer 7 on a surface of the multi-layered insulating structure using an ALD process, as taught by Zheng, in place of thermal oxidation because: the coverage of the liner insulating layer formed by ALD is conformal over the entire surface of the trench and multi-layered structure, including the groove. That is, the thickness of the liner layer over the entire surface of the trench and multi-layered structure, including the groove, is substantially equal.[2]

Zheng does not teach that the liner oxide layer 9 is deposited to a thickness of approximately 100 to 300 Å, as recited in claim 5. However, it

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insulating layer, since intrinsic polysilicon, unlike doped polysilicon, behaves as an insulator.

would have been obvious to one of ordinary skill in the art at the time the invention was made, to deposit the liner oxide layer to a thickness of approximately 100 to 300 Å, since it has been held that where general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (*In re Aller*, 105 USPQ 233).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagatani in view of Zheng as applied to claim1 above, and further in view of Zhang et al. (US 6,284,623 B1).

Nagatani lacks anticipation in not teaching that the multi-layered structure comprises an upper oxide layer, an intermediate nitride layer, and a lower oxide layer. As discussed above, the multi-layered insulating structure comprises a pad oxide layer 2, a polysilicon layer 3, and a silicon nitride layer 4. As shown in fig.1, the polysilicon layer 3 forms an intermediate layer between the pad oxide layer and the silicon nitride layer.

The Zhang et al. patent (Zhang) discloses a method for forming a semiconductor device (figs. 3-10 and accompanying text). The method, which is similar to that of Nagatani, comprises: forming a multi-layered insulating structure on a semiconductor substrate 302, wherein the multi-layered insulating structure comprises an upper oxide layer 308, an intermediate nitride layer 306, and a lower oxide layer 304 (fig.3 and col. 3, line 7-39); forming an opening in the insulating structure, and forming a trench in the

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[2] It is well known in the art that layers deposited using ALD have excellent conformality.

semiconductor substrate (fig. 4 and col. 3, line 59 - col. 4, lines 4); forming a groove 502 on an edge portion of the intermediate layer 306 of the multi-layered insulating structure (fig. 5 and col. 4, lines 12-17); forming a liner insulating layer 604 in a desired thickness on a surface of the multi-layered insulating structure (fig. 6 and col. 4, lines 41-47); and filling the groove and the trench with an oxide layer 702 (fig. 7 and col. 5, lines 5-7).

Since Nagatani and Zhang are from the same field of endeavor - methods of making shallow trench isolation structures in semiconductor devices - the purpose for which Zhang is relied upon would have been recognized in the pertinent reference of Nagatani by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Nagatani and Zheng by forming the multi-layered insulating structure comprising an upper oxide layer, an intermediate nitride layer, and a lower oxide layer, as taught by Zhang, because: depending on the etchant used, the nitride intermediate layer will etch faster than the upper and lower oxide layers, thereby forming a groove at an edge portion of the intermediate layer of the multi-layered structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The

fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMJ
14 November 2004

Mary Wilczewski
Primary Examiner